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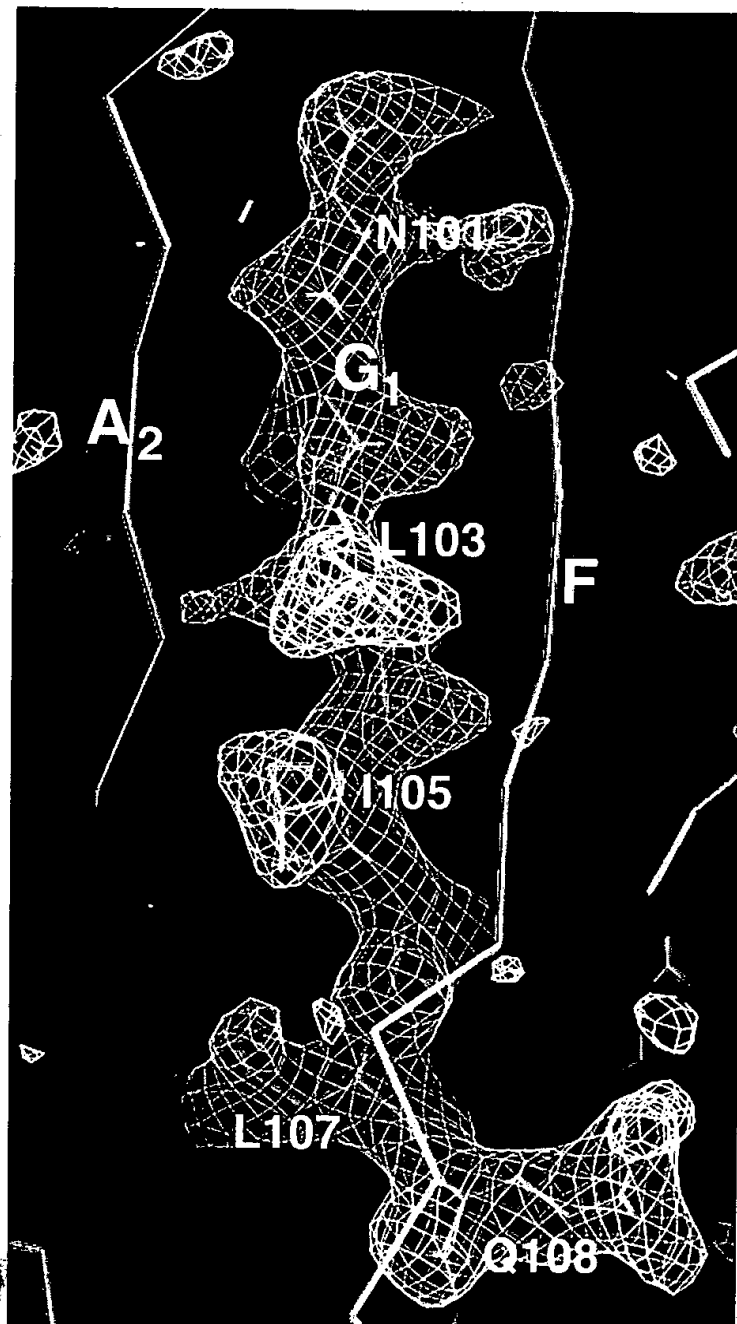
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APPROVED	O.G. FIG.	
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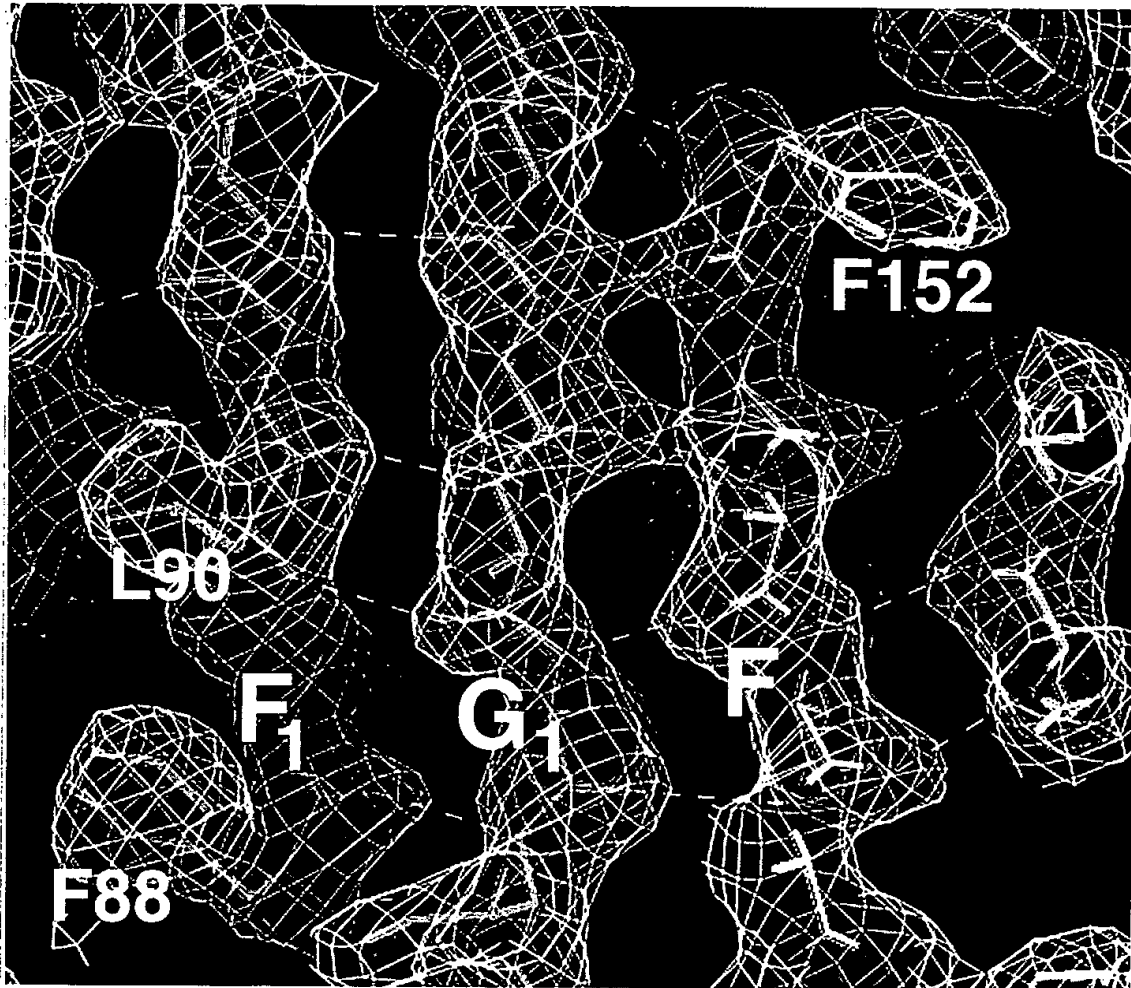
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FIG. 1A



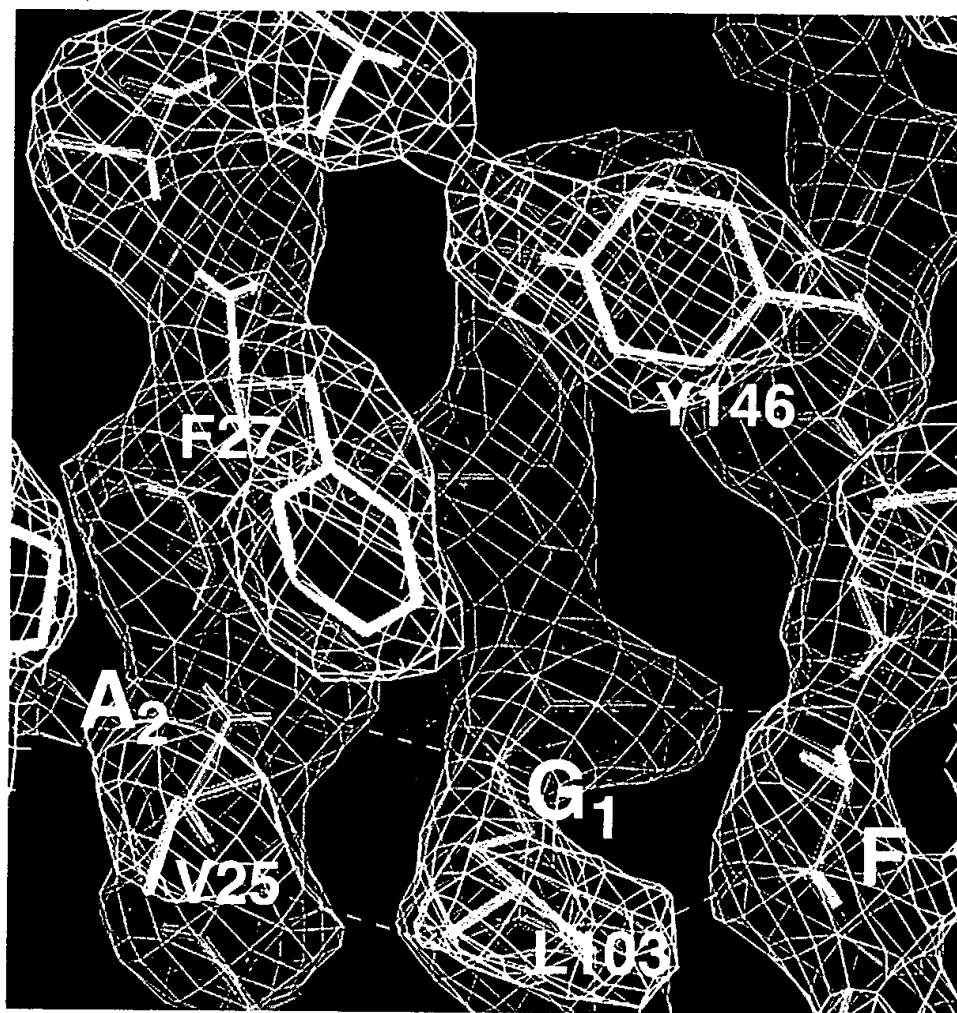
APPROVED	O.G. FIG.	
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FIG. 1B



APPROVED	O.G. FIG.	
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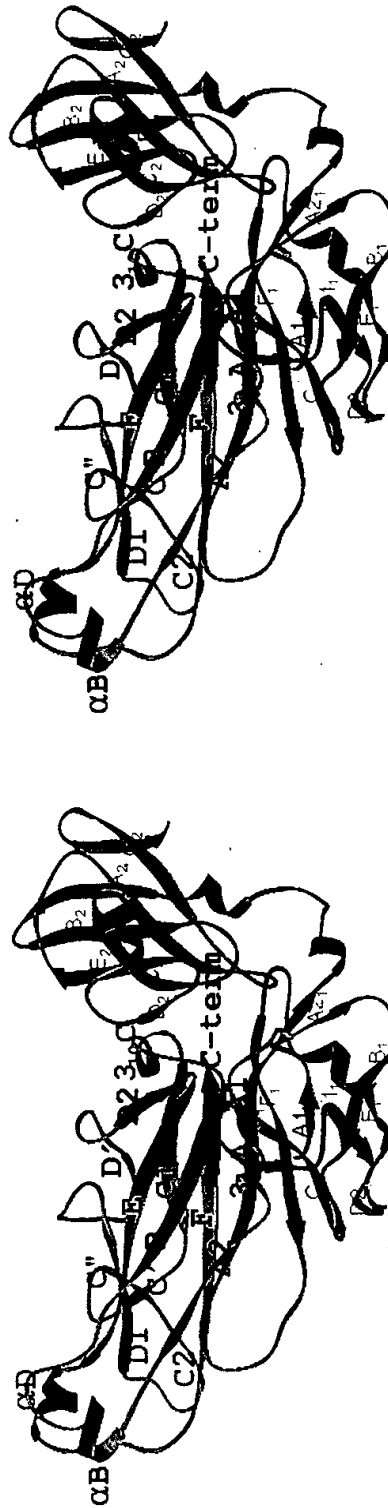
FIG. 1C



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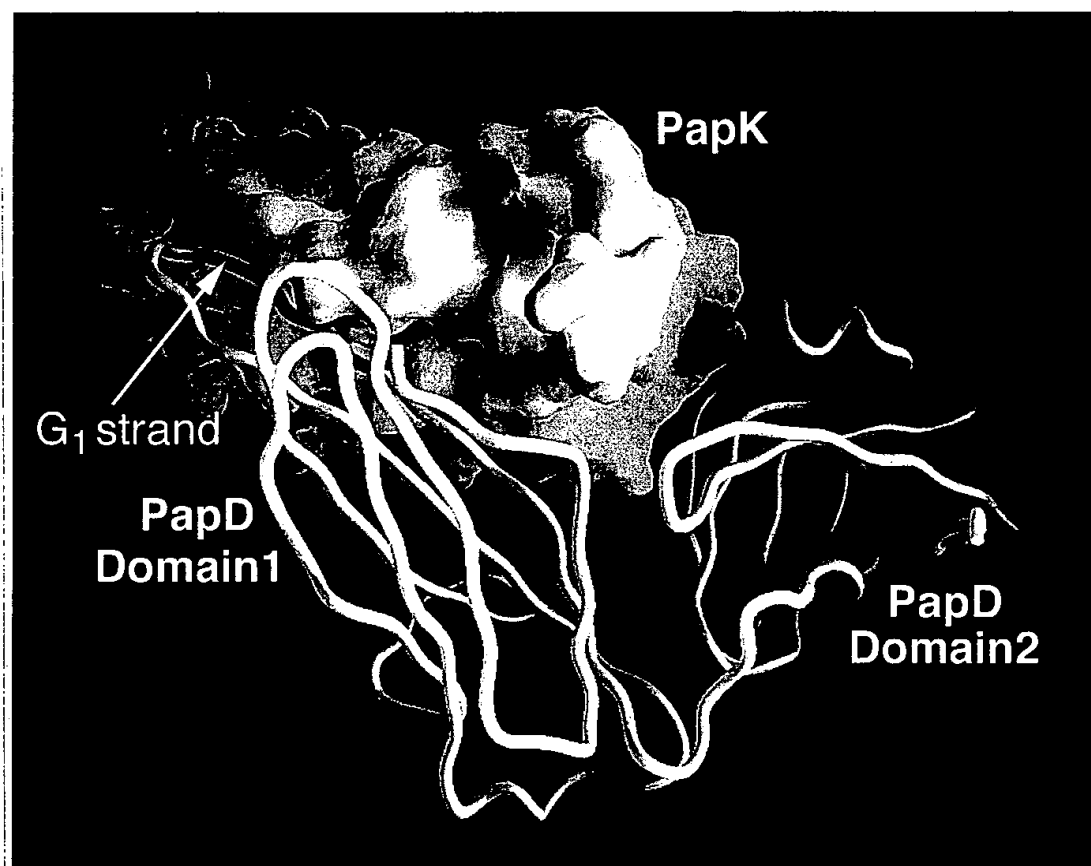
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FIG. 2A



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FIG. 2B

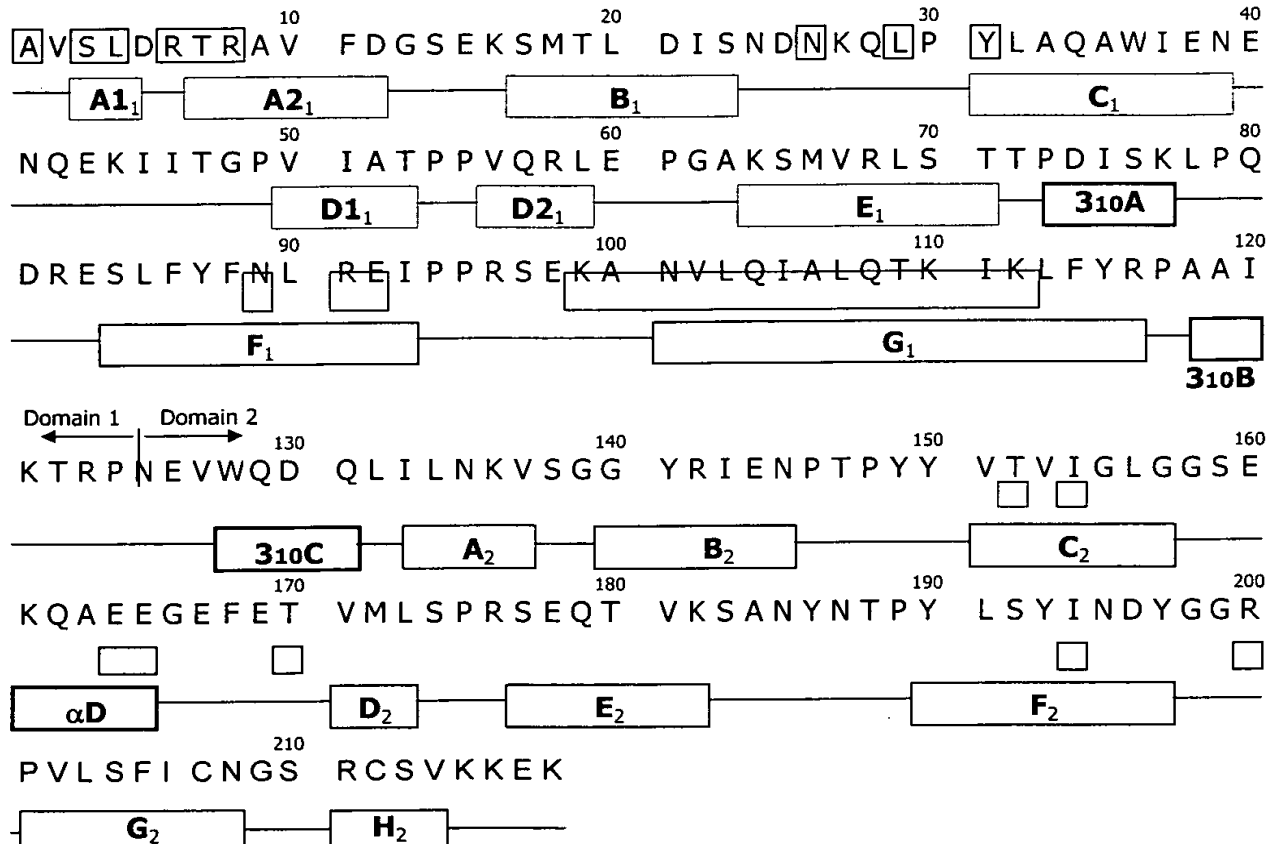


APPROVED	C.G. FIG.	
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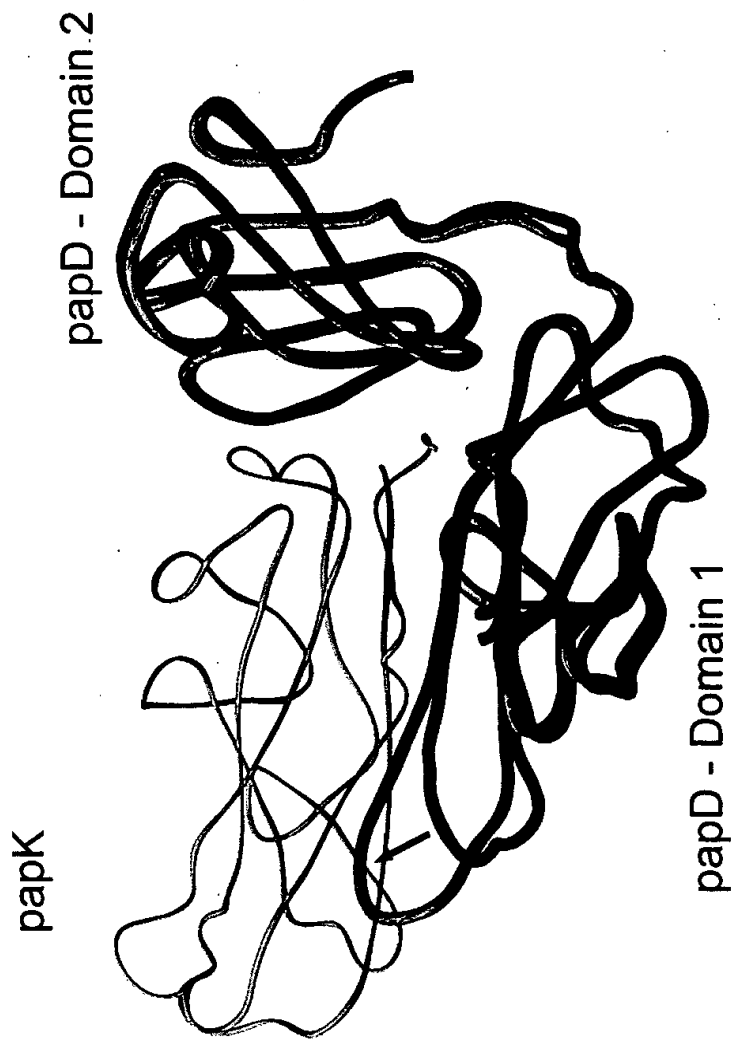
FIG. 3C



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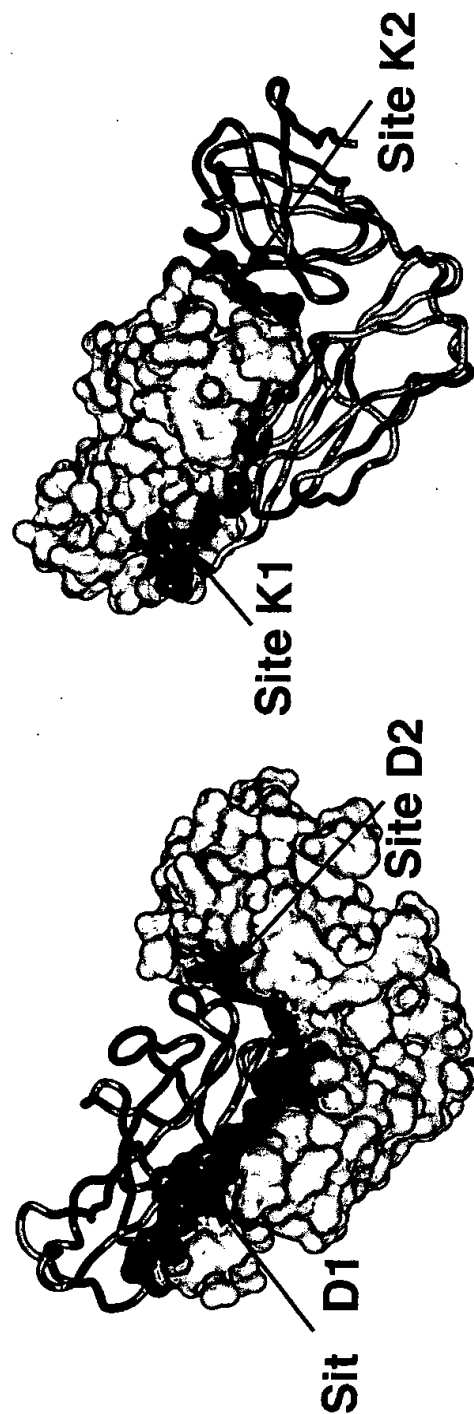
APPROVED	O.G. FIG.	
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FIG. 4



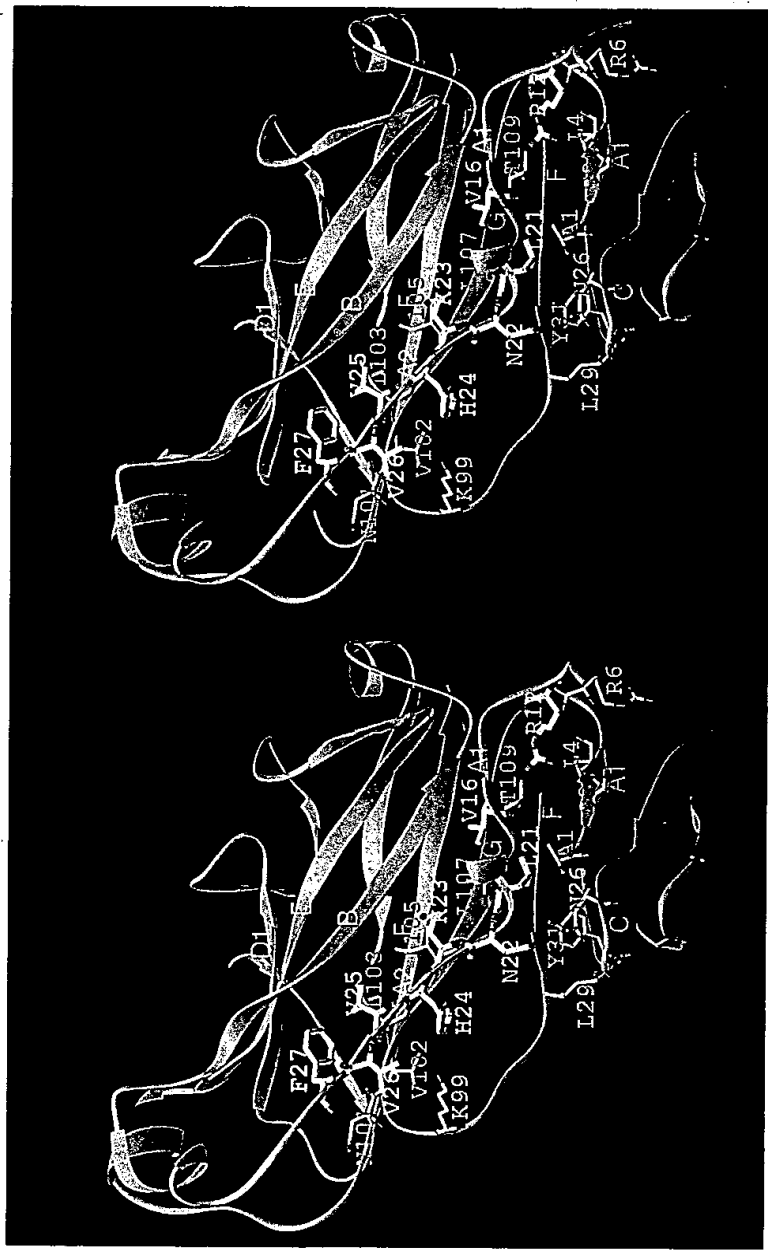
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FIG. 5



APPROVED	J.G. FIG.	
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FIG. 6A



APPROVED	C.S. FIG.	
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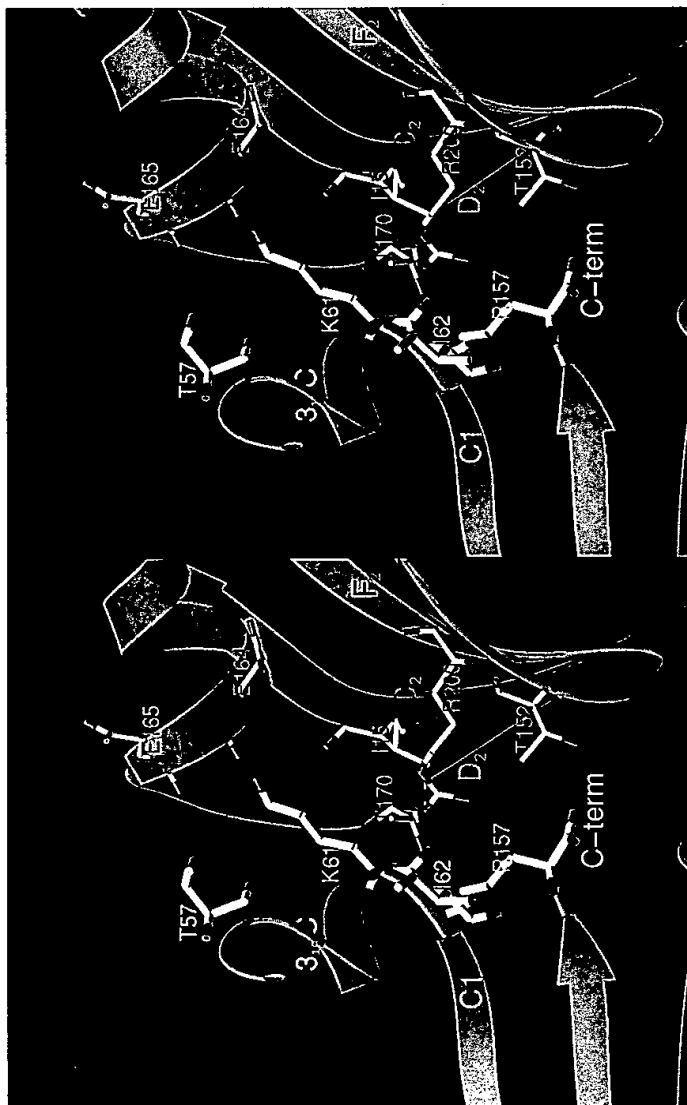
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FIG. 6B



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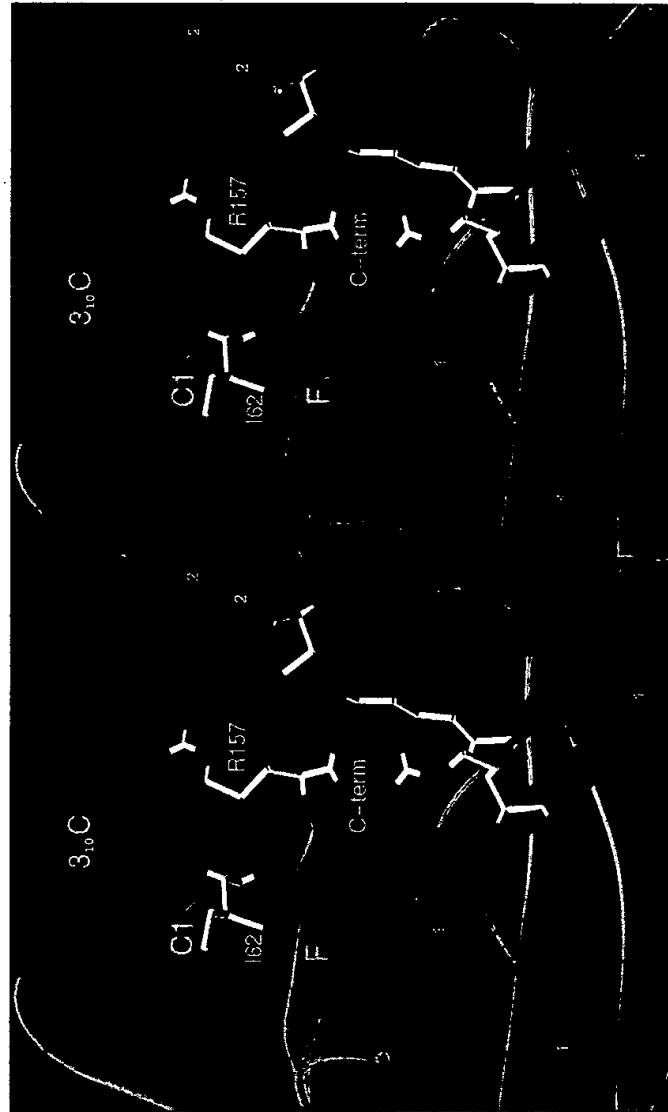
FIG. 6C



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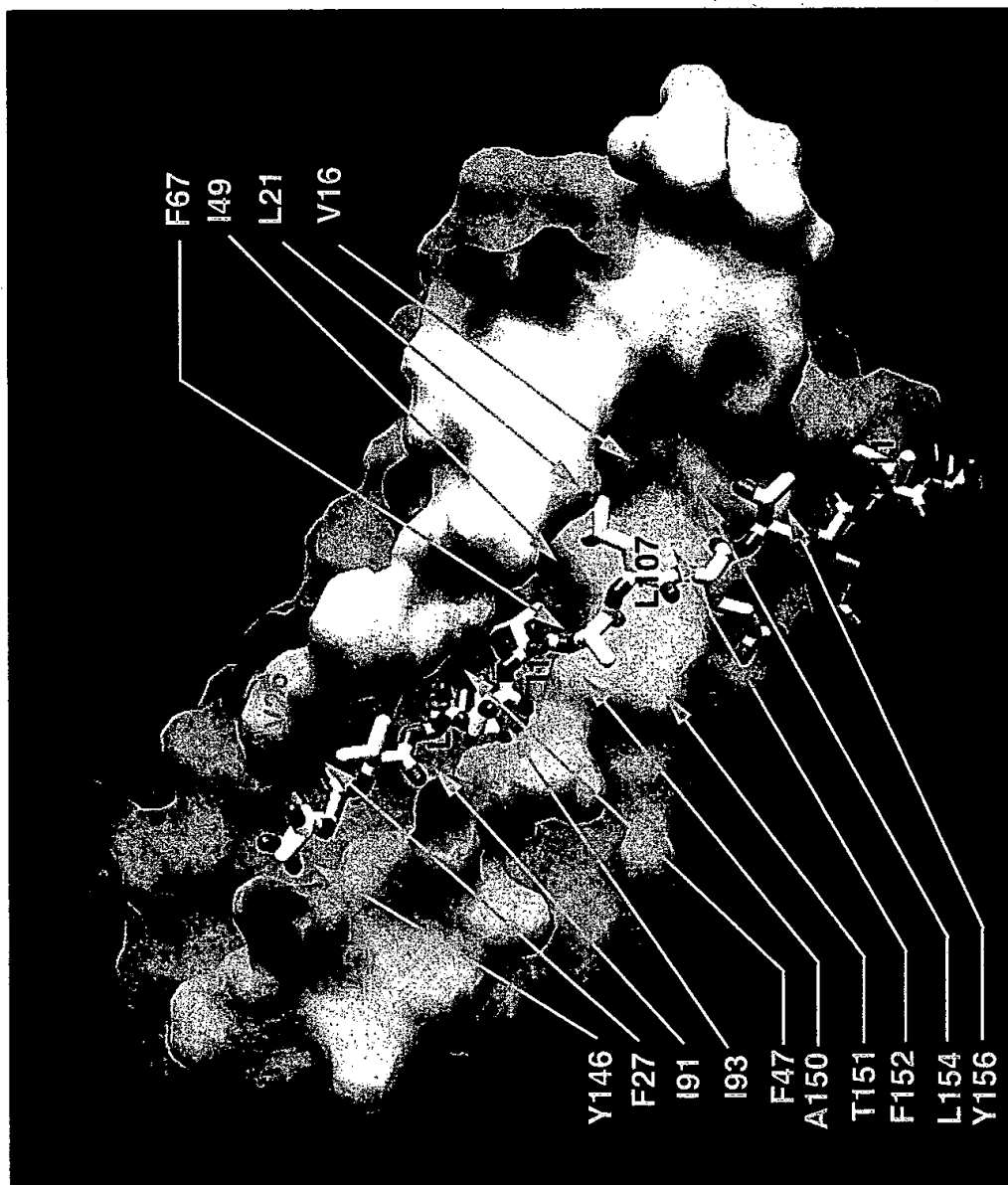
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FIG. 6D



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FIG. 6E



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FIG. 7B

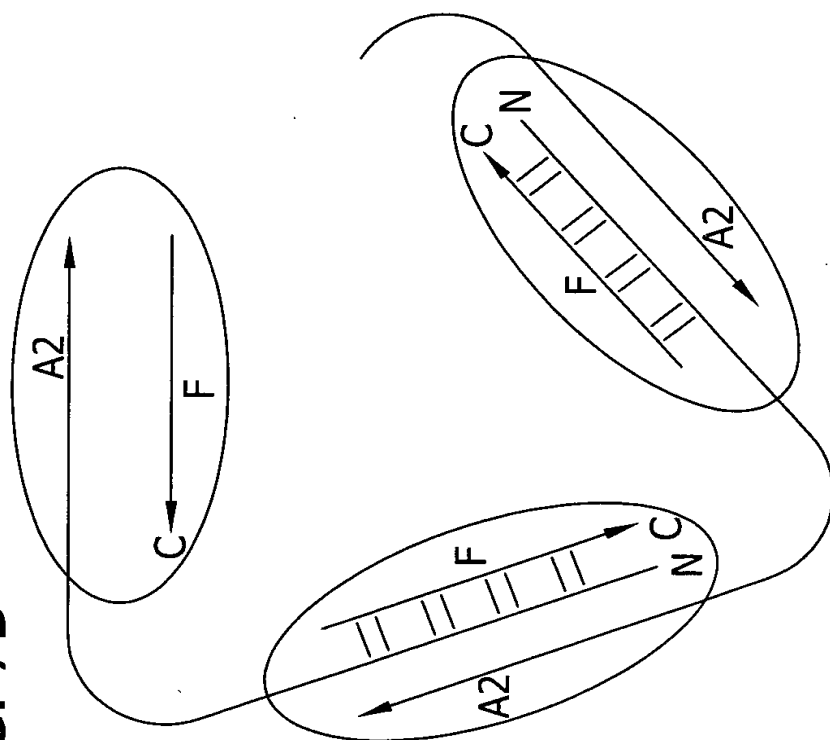
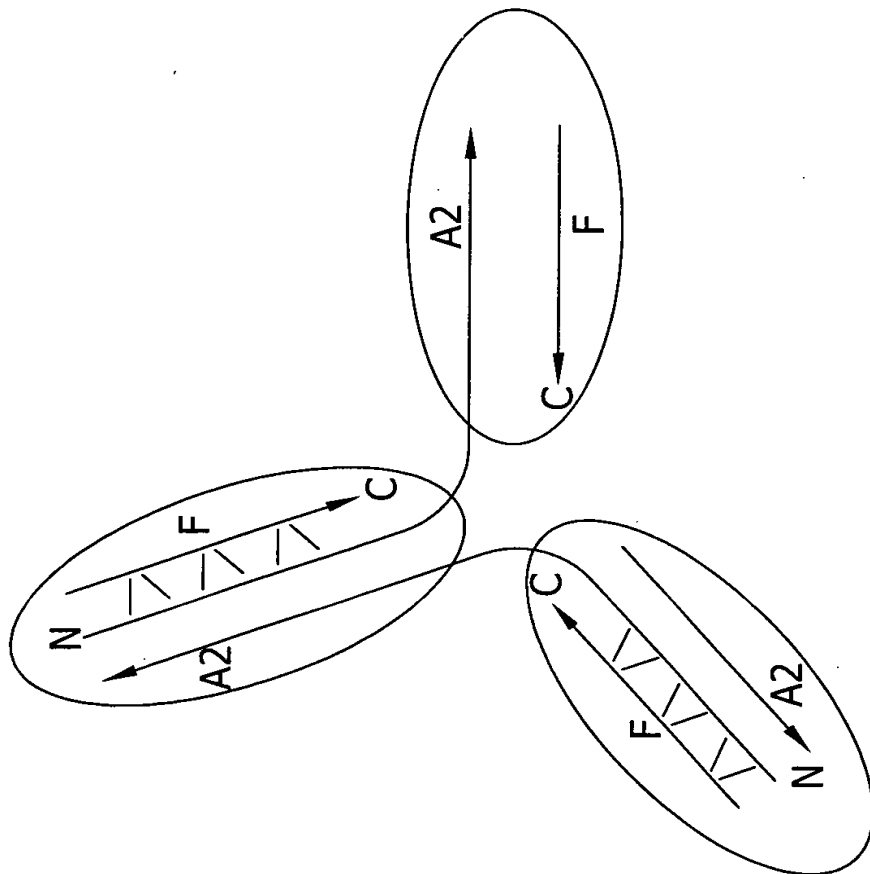
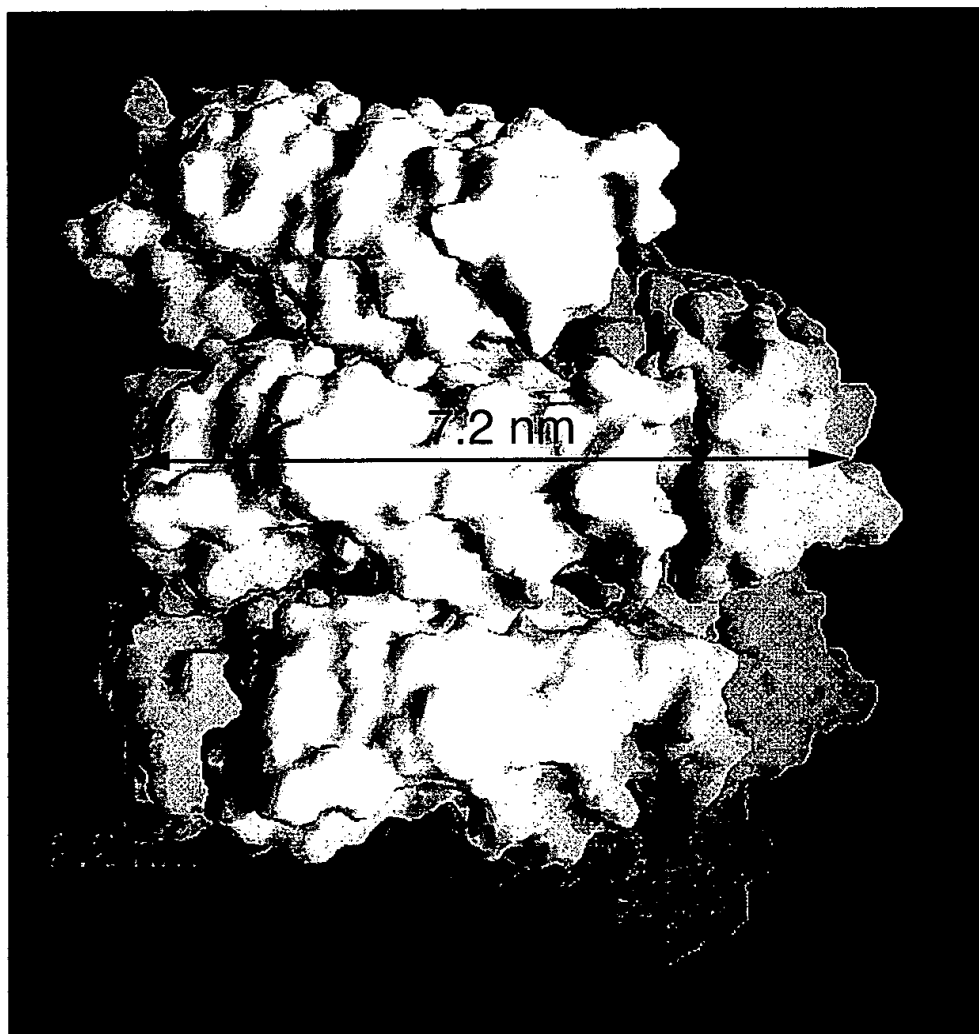


FIG. 7A



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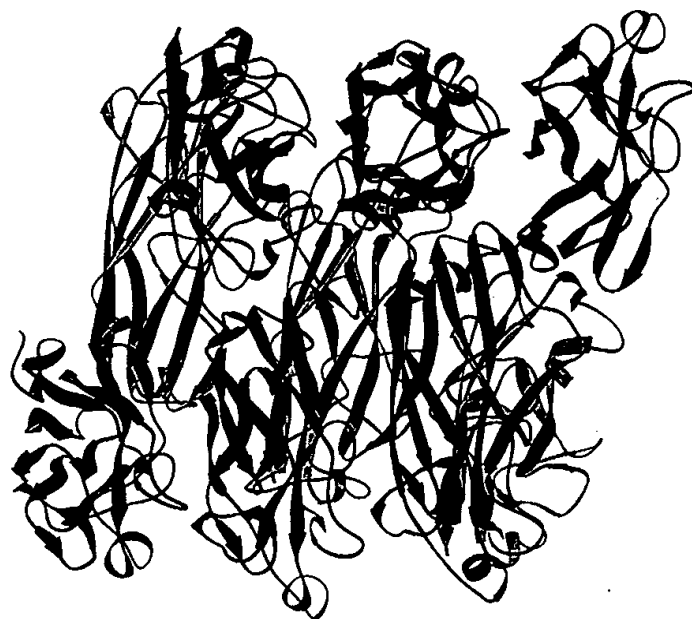
FIG. 7C



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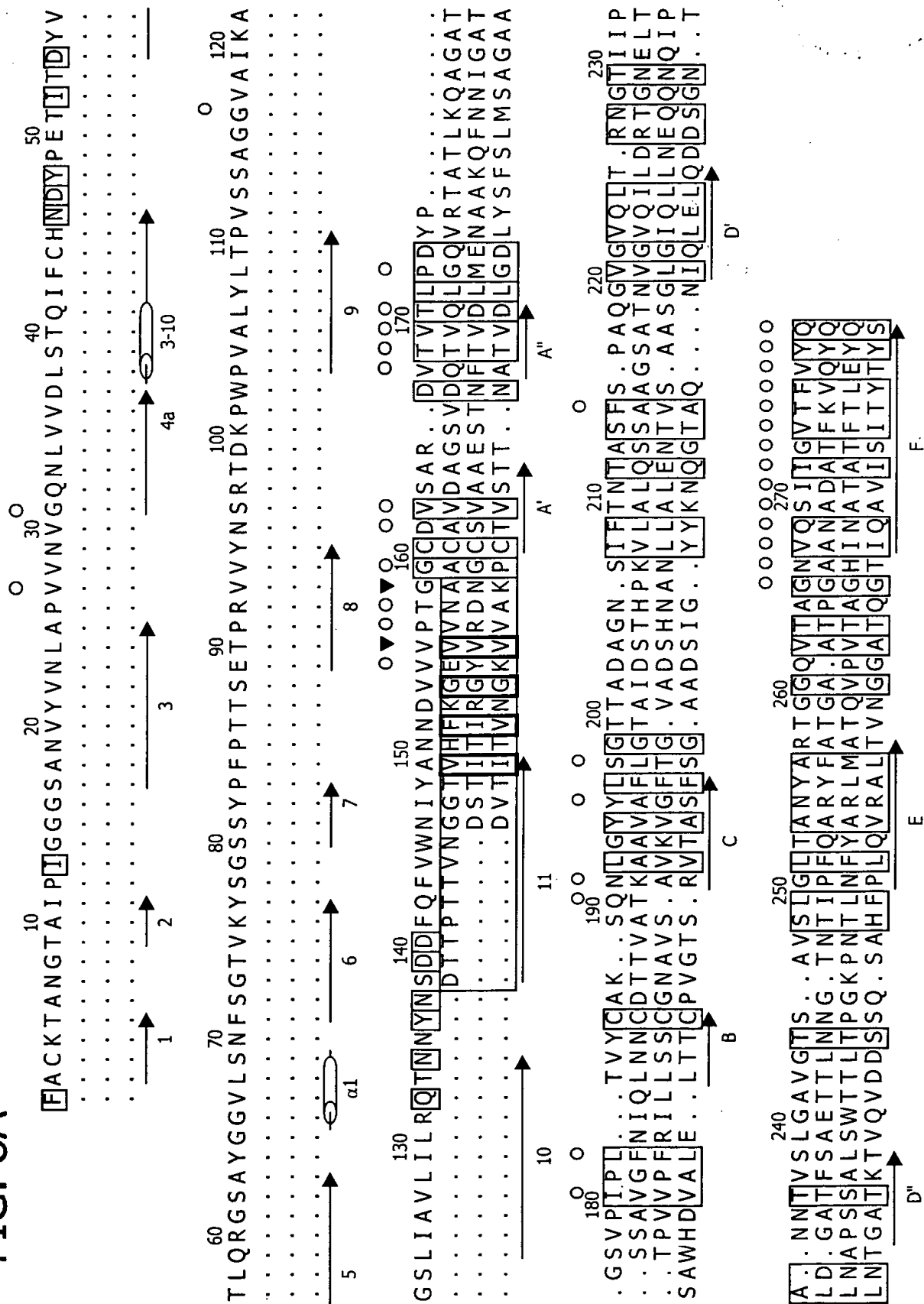
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FIG. 7D



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FIG. 8A



A diagram of a 10-bit shift register. It consists of ten horizontal bars, each representing a bit cell, labeled 1 through 10 from bottom to top. Each bar has an arrow at its right end indicating the direction of data flow. The arrows for cells 1 through 9 point to the right, while the arrow for cell 10 points to the left. Feedback loops are shown as curved lines connecting the outputs of cells 4, 6, 7, 8, and 10 back to the input of cell 1. Specifically, the loop from cell 4 goes to the top of cell 1; the loop from cell 6 goes to the top of cell 1; the loop from cell 7 goes to the top of cell 1; the loop from cell 8 goes to the top of cell 1; and the loop from cell 10 goes to the top of cell 1.

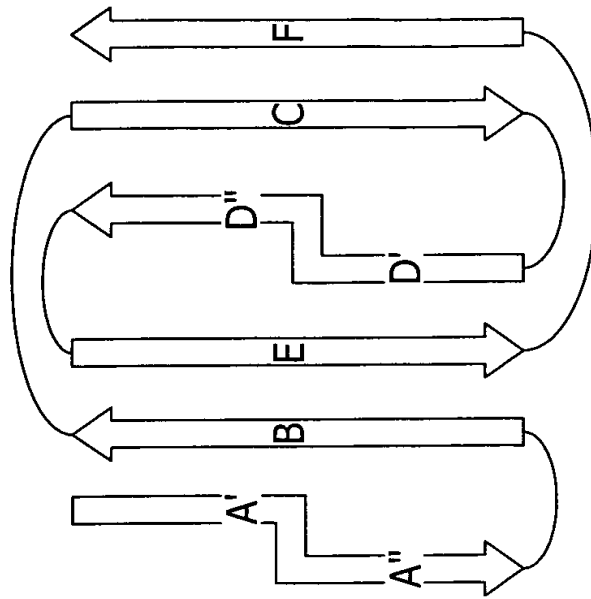


FIG. 9A

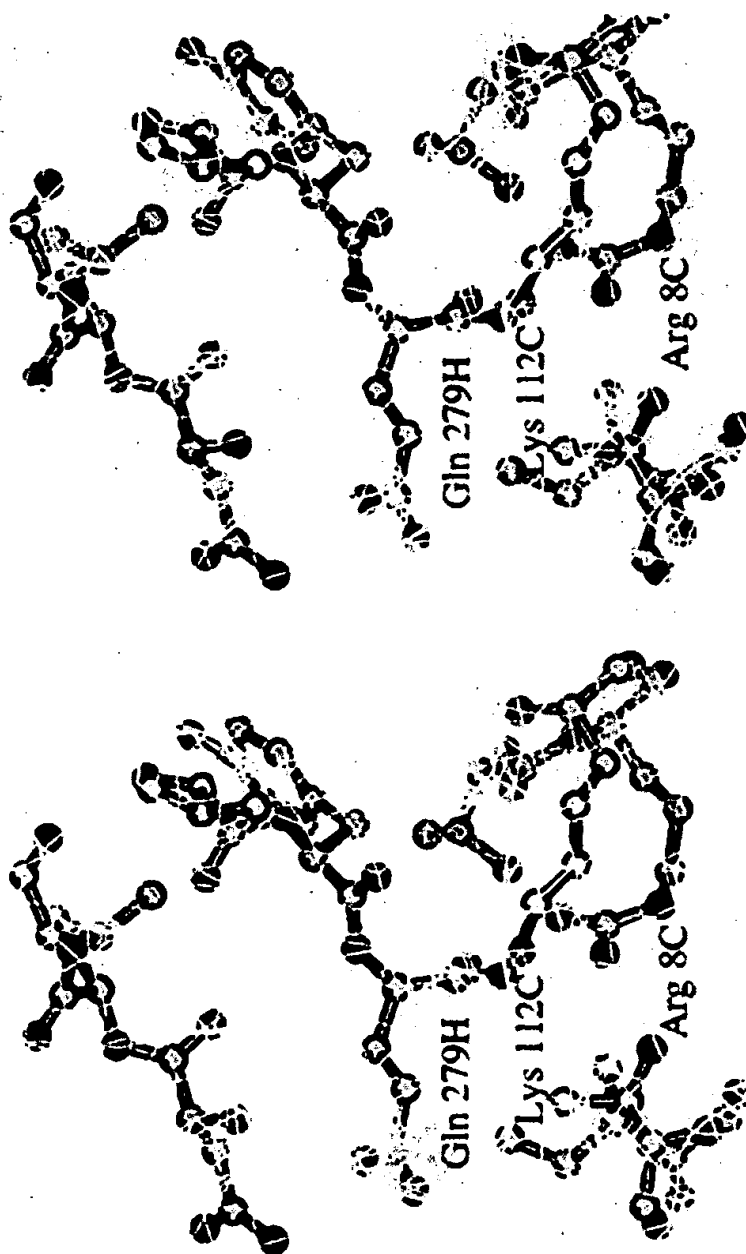
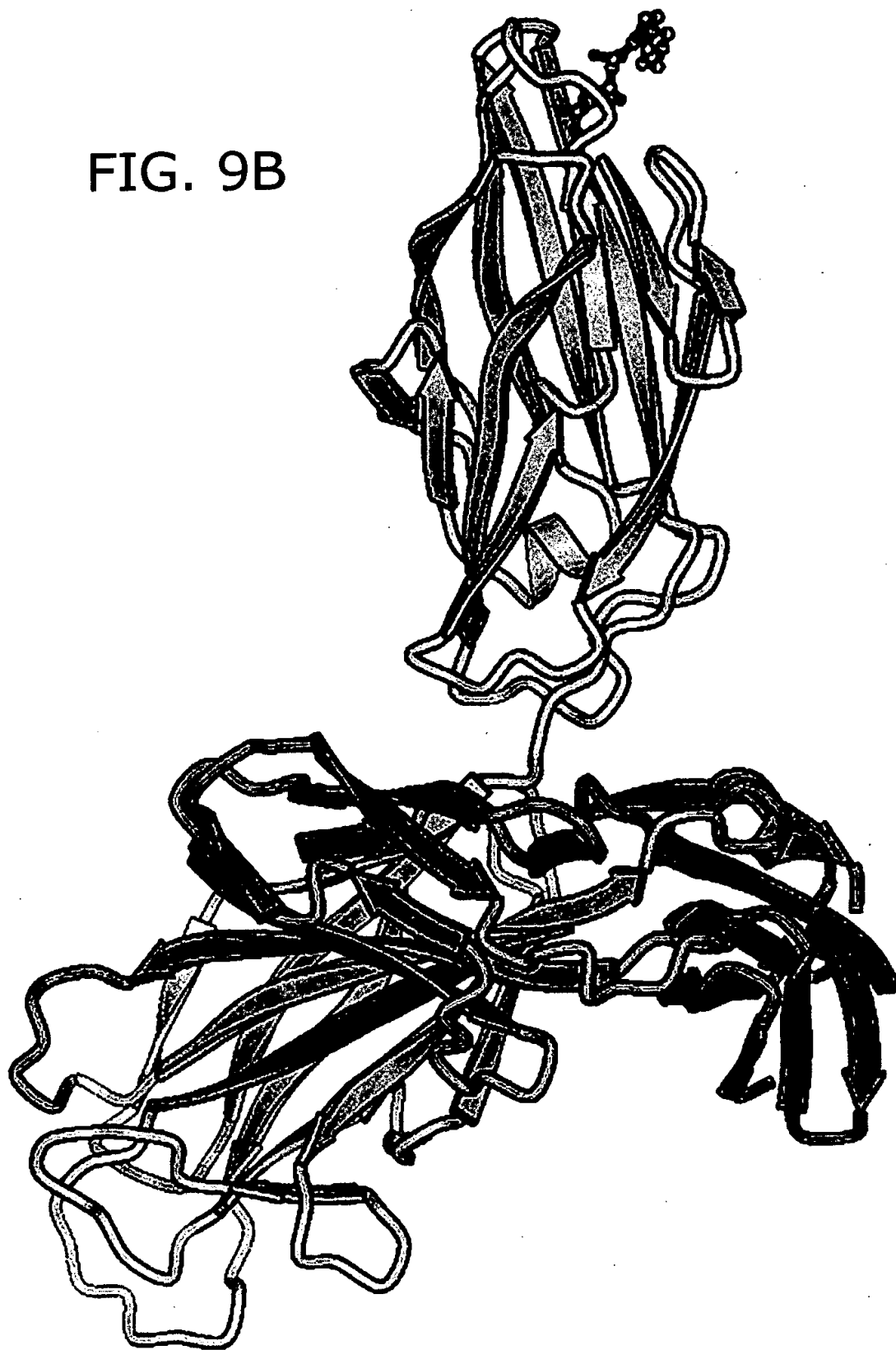
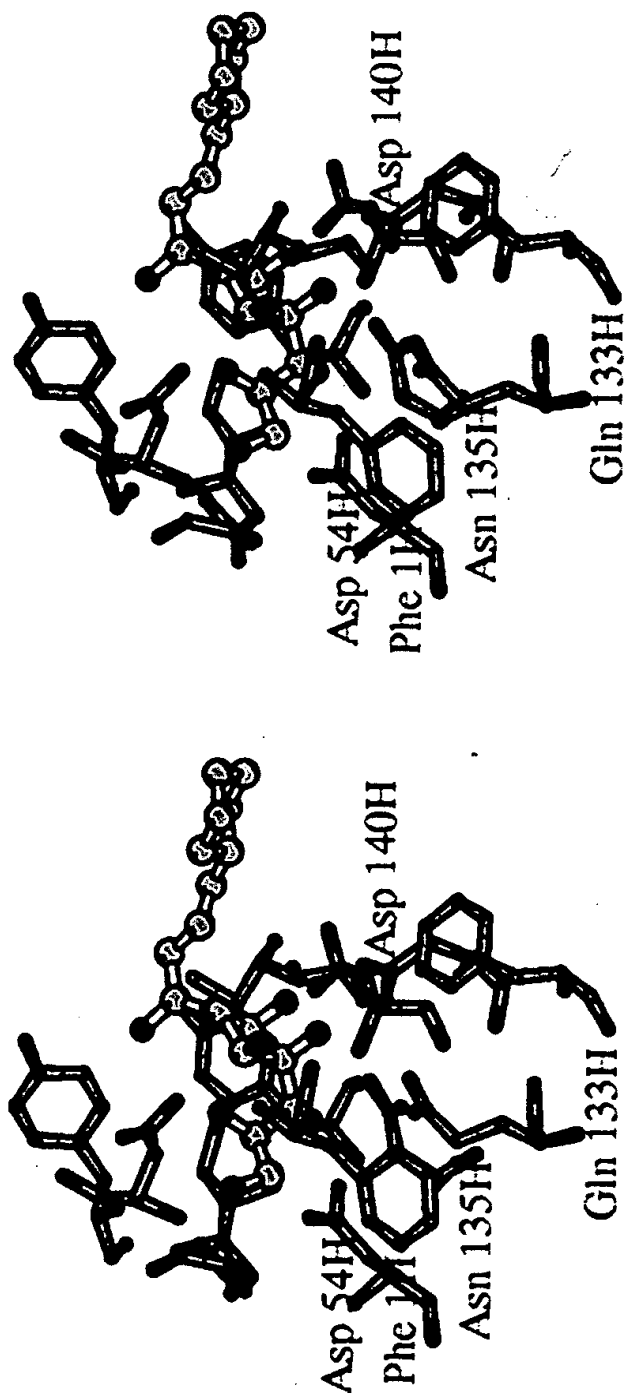


FIG. 9B



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FIG. 10A



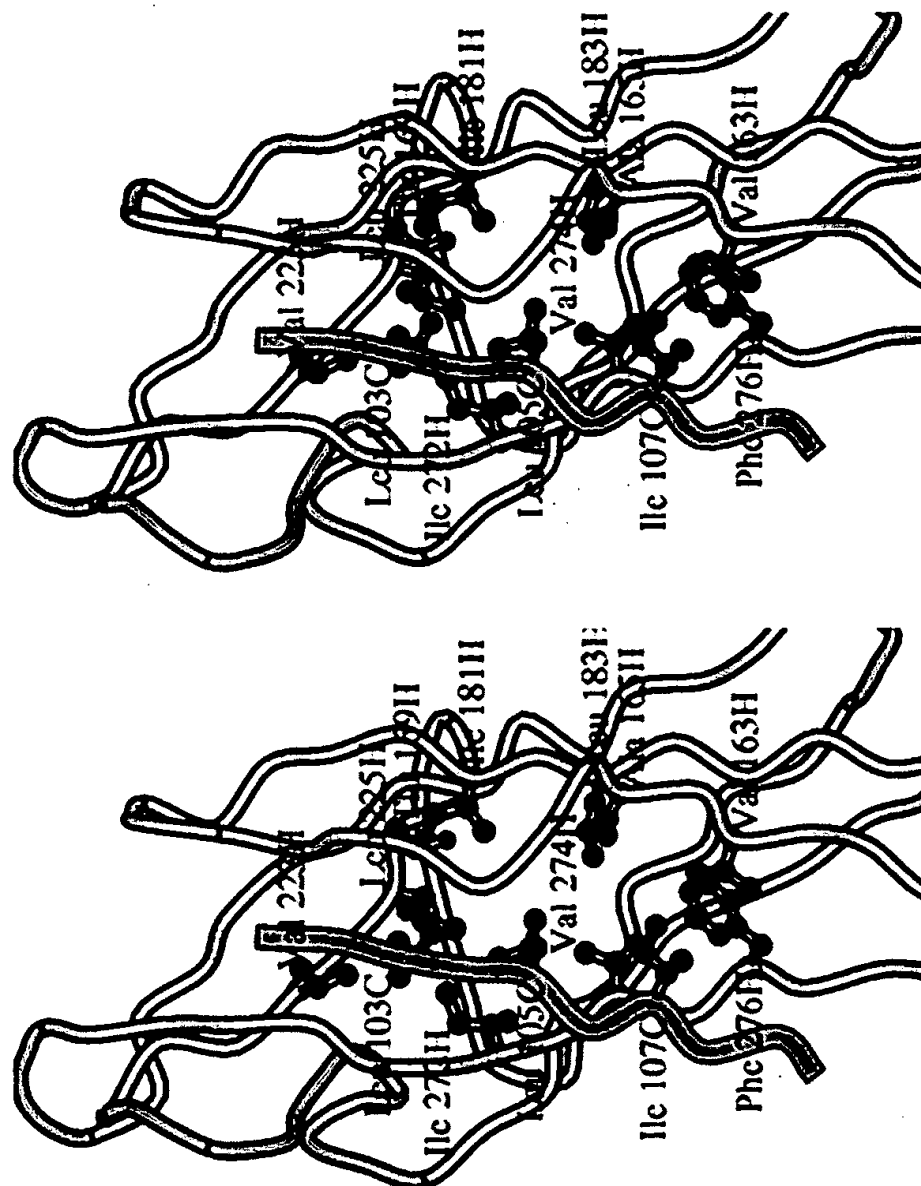
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FIG. 10B



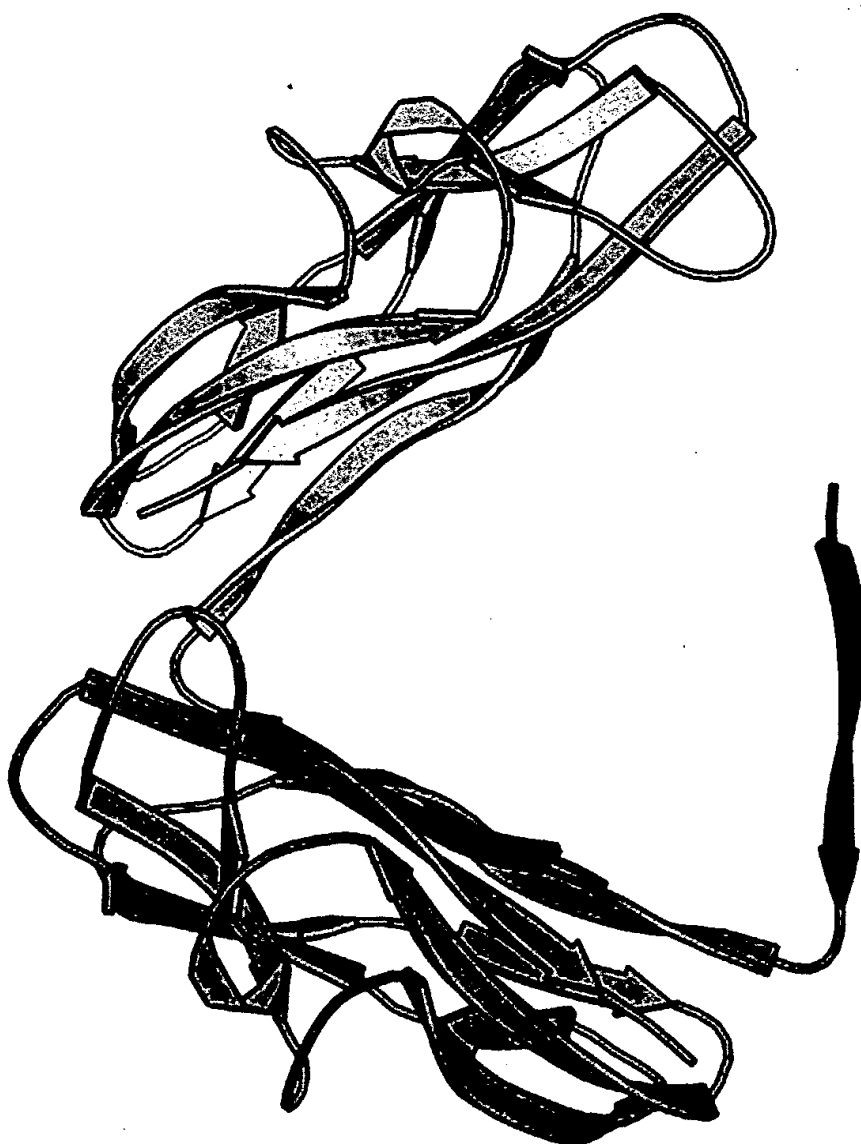
APPROVED	J.G. FIG.	
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FIG. 10C



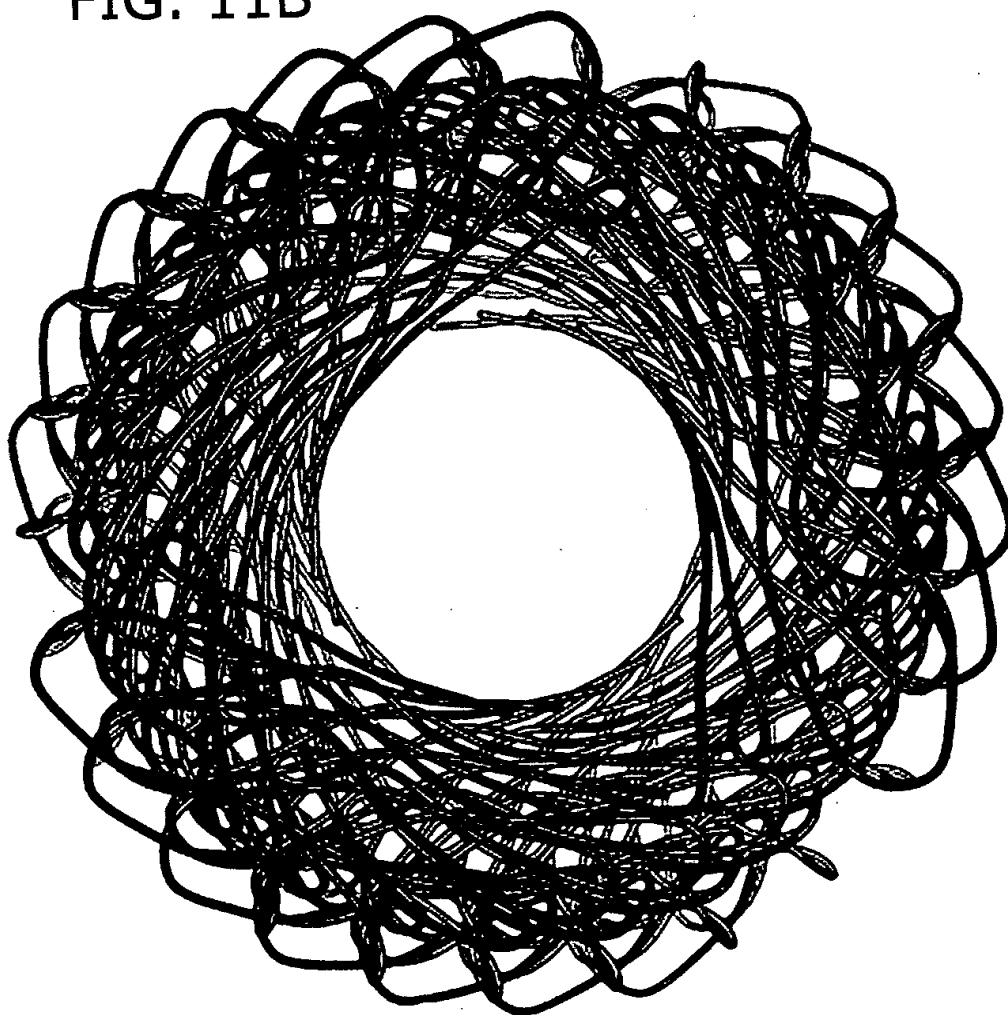
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FIG. FIG.		
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FIG. 11A



APPROVED 10.G. FIG.	
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FIG. 11B



APPROVED	D.G. FIG.	
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FIG. 11C



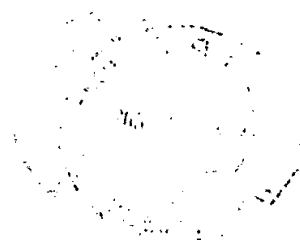


FIG. 12

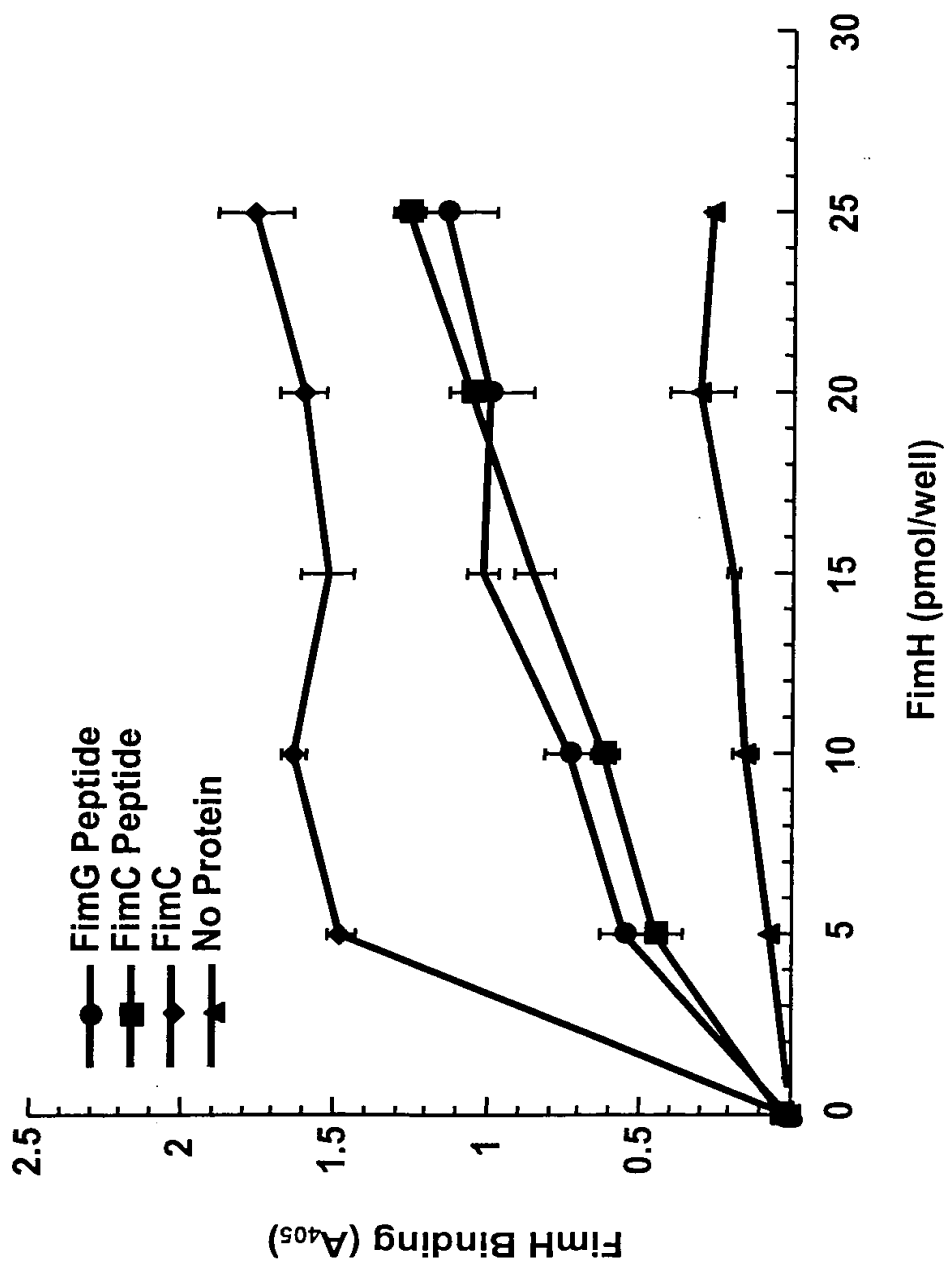


FIG. 13

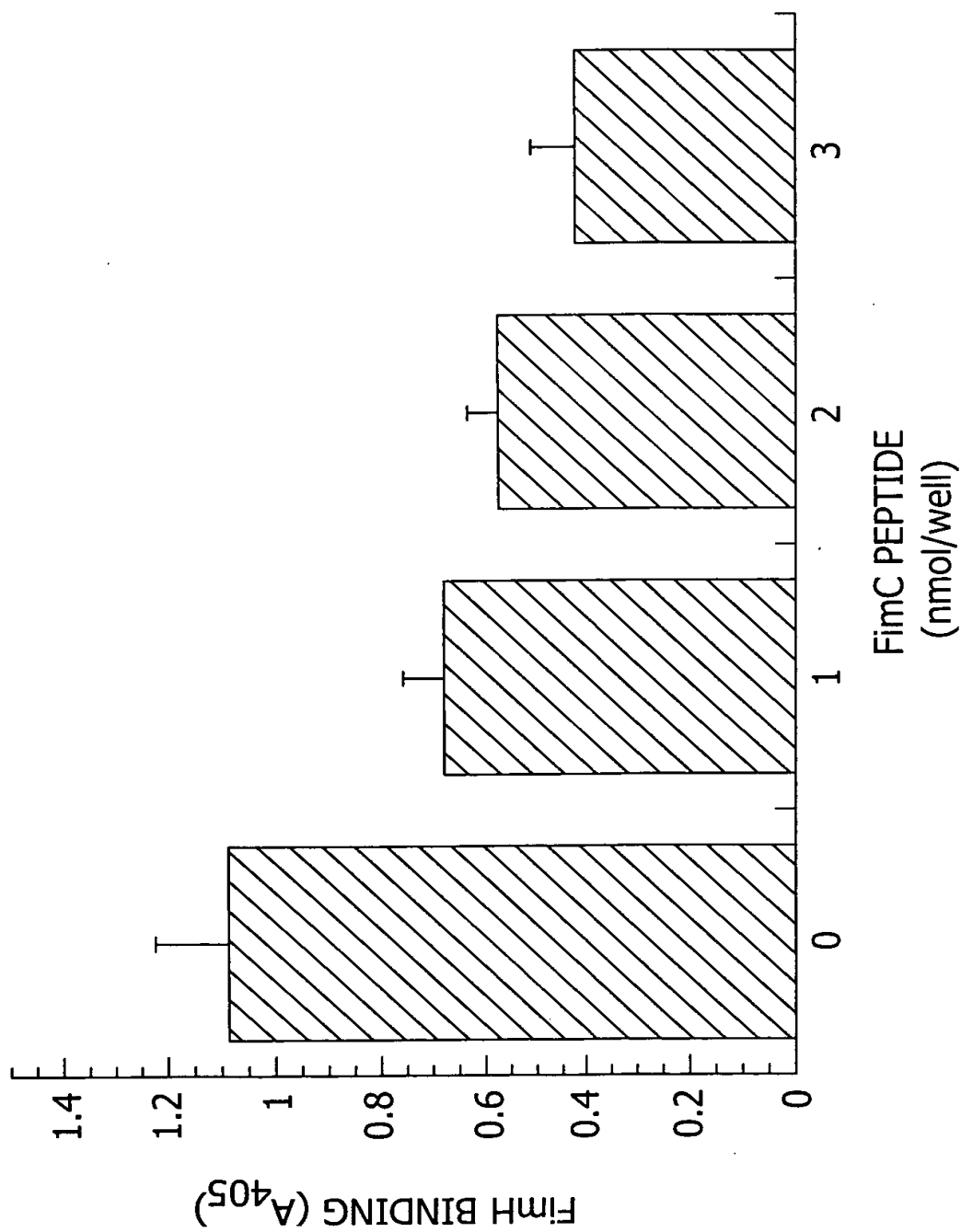




FIG. 14

